Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A method for concurrently routing frames through a switch wherein each of the frames is formatted with one of a plurality of formats, the method comprising:

identifying the format of each of the frames, ~~and~~

controlling the operation of the switch with reference to the format of each of the frames,

tracking a connection state of the switch with reference to the format of each of the frames, and

storing the connection state in a memory register.

2. (Previously Presented) The method as recited in claim 1 wherein the switch is configured with connection states and wherein each of the frames has a first format or a second format and wherein the controlling includes controlling the connection states of the switch so that a frame with the first format has precedence over a frame with the second format.

3. (Original) The method as recited in claim 2 wherein the first format contains a single large packet and the second format contains a plurality of small packets, the identifying including determining if each of the frames is of the first format or the second format.

4. (Original) The method as recited in claim 2 wherein the controlling includes latching the connection states of the switch for a duration corresponding to each of the frames if at least one of the frames has the first format.

5. (Original) The method as recited in claim 2 wherein the controlling includes locking the connection states of the switch for each of a series of durations corresponding to sub-durations of each of the frames if the frames are only of the second format.

6. (Original) The method as recited in claim 1 further including additional switches so that all switches form interconnected switches, the identifying including identifying at each of the additional switches the format of each of the frames, and the controlling including controlling the operation of each of the additional switches with reference to the format of each of the frames.

7. (Previously Presented) A method for operating a switch configured with connection states, the method comprising:

defining a dual-format frame for concurrently routing a plurality of frames through the switch,

identifying at the switch the format of each of the frames, and

controlling the connection states of the switch with reference to the format of each of the frames.

8. (Original) The method as recited in claim 7 wherein the dual-format includes a first format containing a single large packet and a second format containing a plurality of small packets and the controlling includes latching the connection states of the switch for a duration corresponding to the large packet if at least one of the frames has the first format.

9. (Original) The method as recited in claim 7 wherein the dual-format includes a first format containing a single large packet or a second format containing a plurality of small packets and the controlling includes locking the connection states of the switch for each of a series of durations corresponding to each of the small packets if the frames are only of the second format.

10. (Previously Presented) A method for concurrently routing two incoming frames through a switch configured with connection states and wherein each of the incoming frames has either a first format containing a single large packet or a second format containing a plurality of small packets, the method comprising:

(a) upon the start of the frames, unlatching the connection state of the switch,

(b) determining if at least one of the frames contains a large packet; if not, continuing with (e),

(c) latching one of the connection states based upon data in the large packet,

(d) transmitting the data in the large and small packets, and then proceeding to (a),

(e) locking the connection state based upon data in the small packets,

(f) transmitting the data in the small packets,

(g) receiving a frame or slot clock signal and, if the signal is from the frame clock, proceeding to (a), and

(h) unlocking the connection state and returning to (e).

11. (Currently Amended) A switch for concurrently routing frames wherein each of the frames is formatted with one of a plurality of formats, the switch comprising:

a means for identifying the format of each of the frames, ~~and~~

a control circuit for controlling the operation of the switch with reference to the format of each of the frames, and

a means for tracking a connection state with reference to the format of each of the frames.

12. (Previously Presented) A switching fabric comprising a multistage interconnection of primitive switches wherein each of the primitive switches is the switch as recited in claim 11.

13. (Original) The switch as recited in claim 11 having connection states and wherein there are two formats including a first format and a second format and wherein the control circuit includes means for controlling the connection states of the switch so that a frame with the first format has precedence over a frame with the second format.

14. (Original) The switch as recited in claim 13 wherein the control circuit includes means for latching the switch for a duration corresponding to each of the frames if at least one of the frames has the first format.

15. (Original) The switch as recited in claim 13 wherein the control circuit includes means for locking the switch for each of a series of durations corresponding to sub-durations of each of the frames if the frames are only of the second format.

16. (Original) The switch as recited in claim 13 wherein the first format contains a single large packet and the second format contains a plurality of small packets and the control circuit includes means for locking the connection states of the switch for each of a series of durations corresponding to each of the small packets if the frames are only of the second format.

17. (Previously Presented) Switching circuitry having: (i) connection state circuitry including connection states for concurrently routing two incoming frames arriving in bits wherein each of the frames is formatted with either a first format or a second format with slots so that either the connection state circuitry is latched for the duration of a frame whenever at least one of the incoming packets has the first format, or the connection state circuitry is locked for each of the slots whenever the frames have only of the second format; and (ii) a frame clock and a slot clock, the switching circuitry further including:

(a) a clock counter for counting bits starting at the signal from either the frame clock or the slot clock,

(b) a latch/lock device for registering one of the connection states,

(c) a first shift register for receiving one of the two incoming frames and a second shift register for receiving the second of the two incoming frames, both registers being responsive to the clock counter,

(d) said connection state circuitry, coupled to the clock counter, the latch/lock device, and the first and second shift registers, further including means for determining said one of the connection states; and

(e) a first multiplexer providing a first output and a second multiplexer providing a second output, both multiplexers being controlled by the connection state circuitry to connect the registers to outputs of the switching circuitry.

18. (Previously Presented) A switching fabric comprising a multistage interconnection of primitive switches wherein each of the primitive switches is the switching circuitry as recited in claim 17.

19. (Previously Presented) A system, in combination with switching circuitry, for concurrently routing two incoming frames arriving in bits wherein each of the frames is formatted with either a first format or a second format used to generate slot clock signals, the switching circuitry including: (a) a clock counter for counting frame clock signals based upon the time duration of each of the frames and bit clock signals based upon the rate of bits conveyed by each of the frames; (b) a first shift register for receiving one of the two incoming frames and a second shift register for receiving the second of the two incoming frames, both registers being responsive to the clock counter; (c) connection state circuitry, coupled to the clock counter and the first and second shift registers, for determining a connection state for the switching circuitry; and (d) a first multiplexer providing a first output and a second multiplexer providing a second output, both multiplexers being controlled by the connection state circuitry to connect the shift registers to the outputs, the system comprising:

a clock counter for counting bit clock signals starting either at the frame clock signals or the slot clock signals, and

a latch/lock device for registering the connection state, the connection state circuitry being latched for the duration of frame whenever at least one of the incoming frames has a first format or being locked for each of the slots whenever the frames are only of the second format.

20. (Previously Presented) A switching fabric comprising a multistage interconnection of primitive switches wherein each of the primitive switches is the system as recited in claim 19.